PRIMENA MIKROKONTROLERA

Analogni komparator

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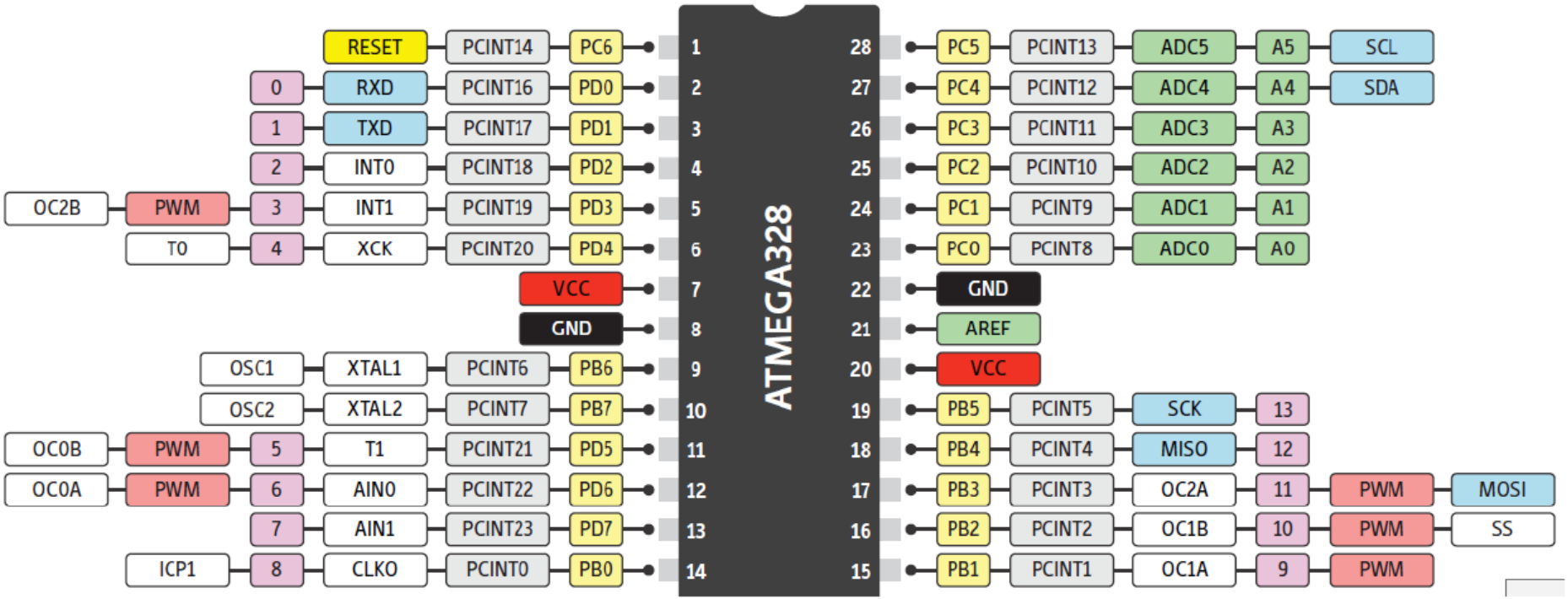
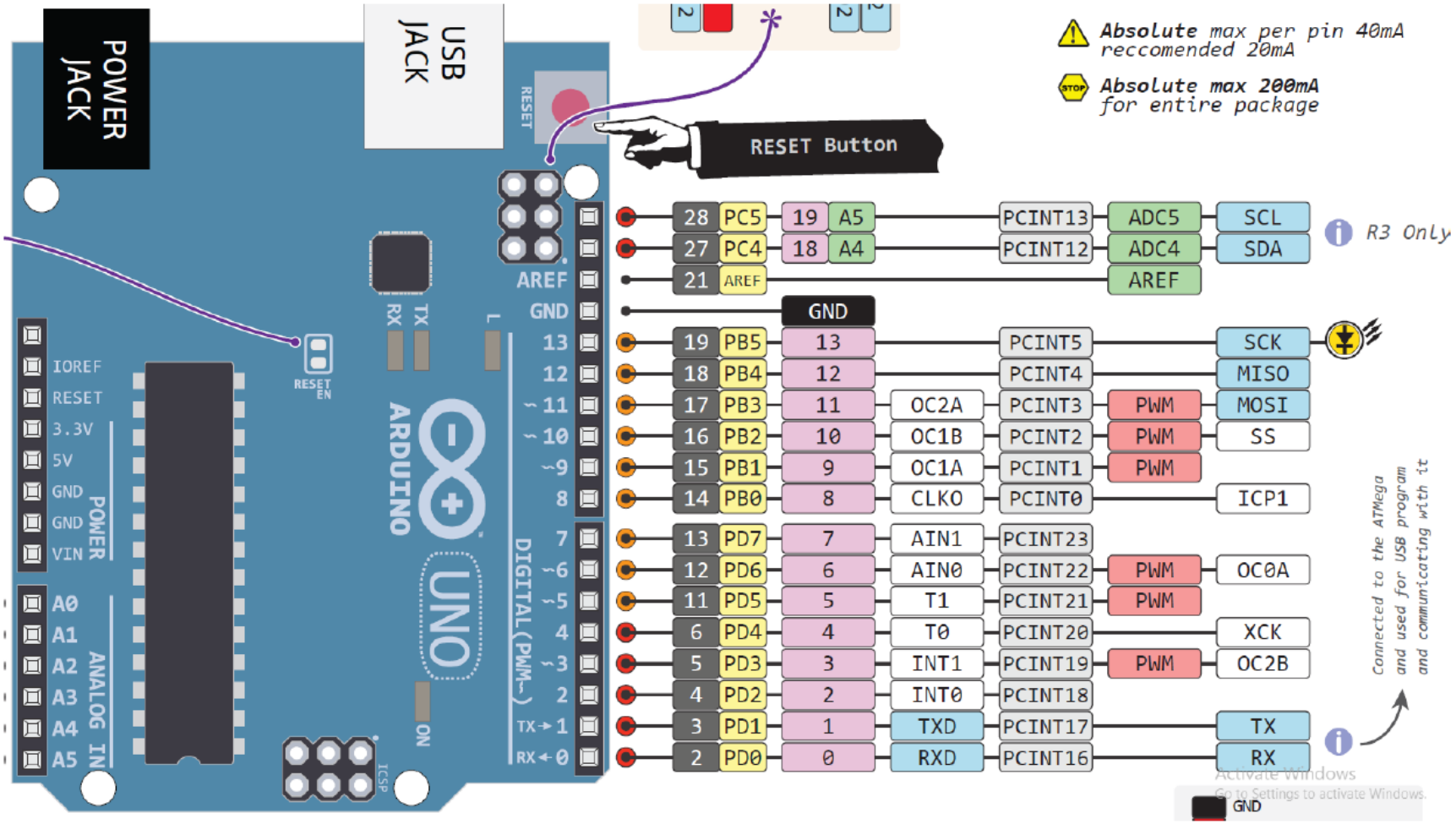
Mikrokontroler ATmega328P



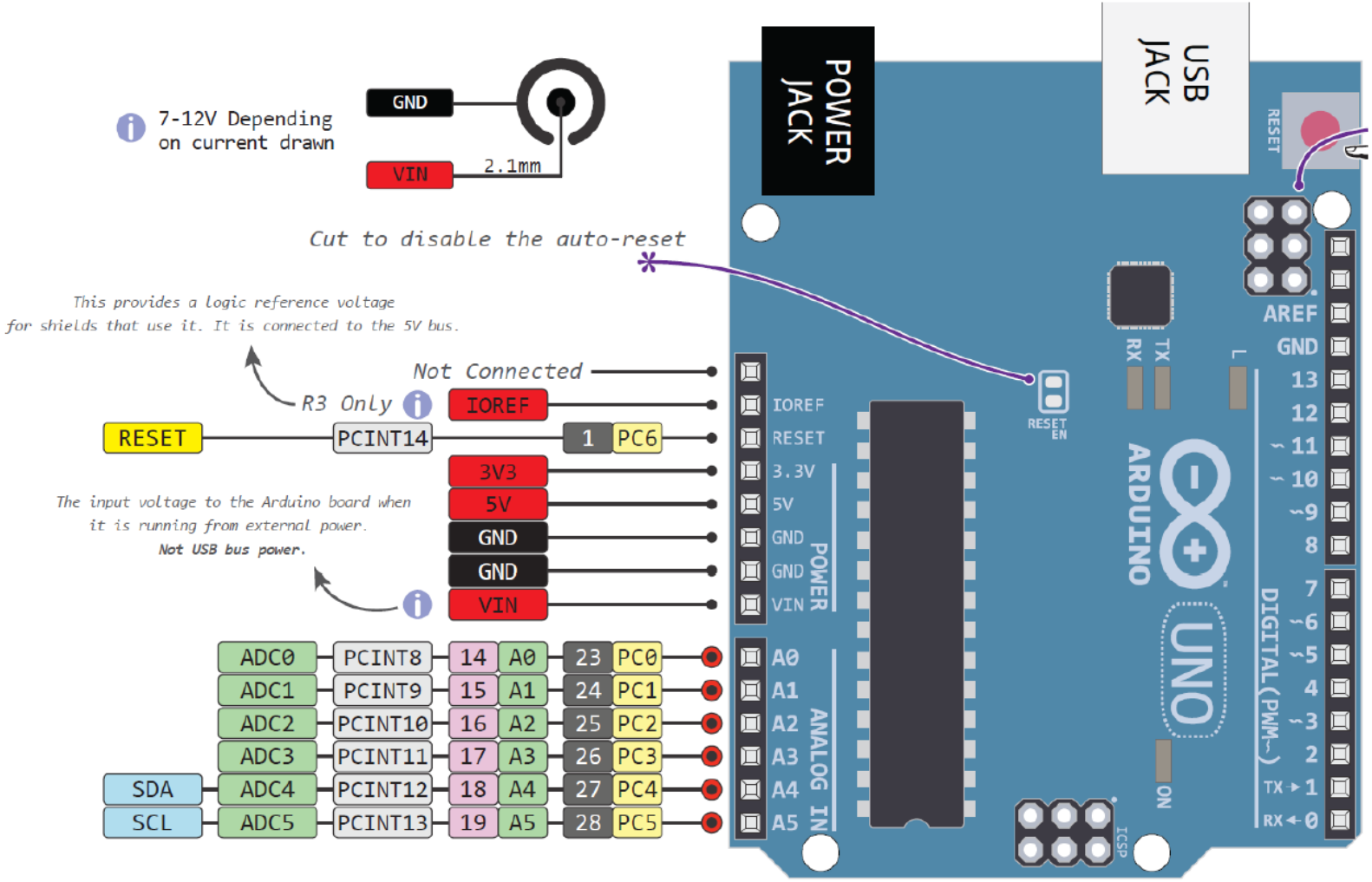
Slika 1. *PINOUT dijagram mikrokontrolera ATmega328P.*

Arduino UNO

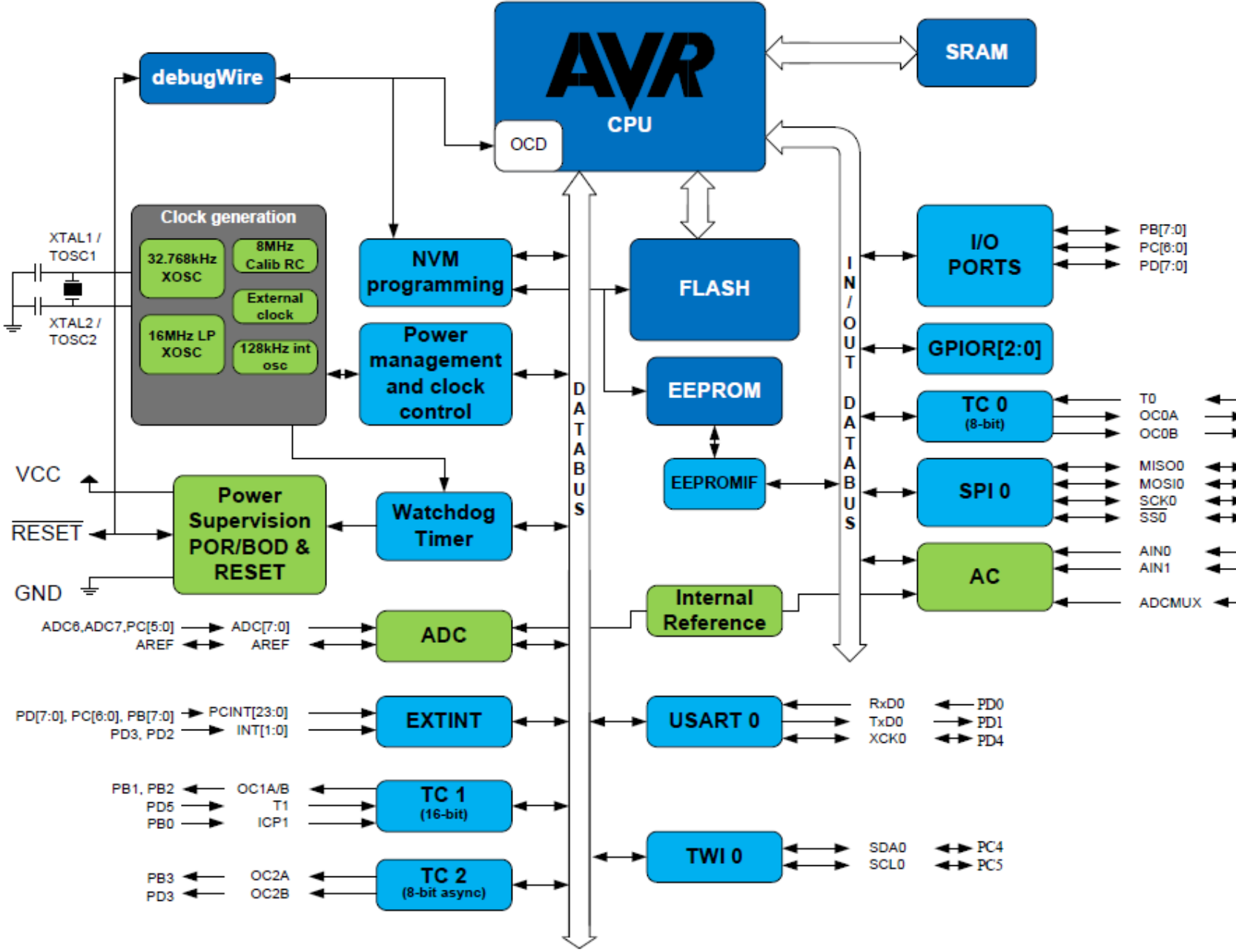


Slika 5. *Deo 2 pinout dijagram Arduino UNO sistema.*

Arduino UNO



Slika 4. *Deo 1 pinout dijagram Arduino UNO sistema.*

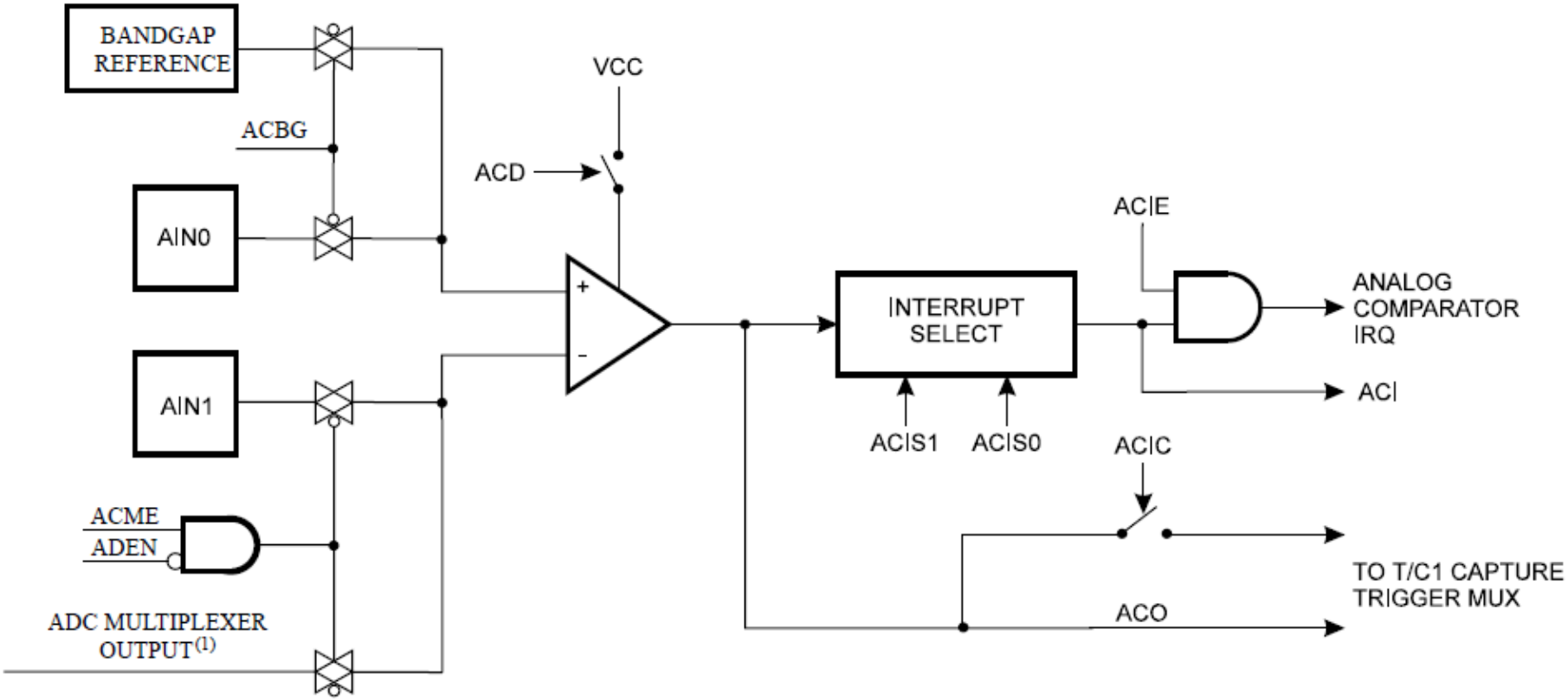

AVR
CPU
OCD
debugWire
SRAM
Clock generation
32.768kHz XOSC
8MHz Calib RC
External clock
16MHz LP XOSC
128kHz int osc
XTAL1 / TOSC1
XTAL2 / TOSC2
NVM programming
Power management and clock control
FLASH
EEPROM
EEPROMIF
DATABUS
I/O DATABUS
I/O PORTS
PB[7:0]
PC[6:0]
PD[7:0]
GPIOR[2:0]
TC 0 (8-bit)
T0
OC0A
OC0B
SPI 0
MISO0
MOSI0
SCK0
SS0
AC
AIN0
AIN1
ADCMUX
VCC
RESET
GND
Power Supervision POR/BOD & RESET
Watchdog Timer
Internal Reference
ADC
ADC6,ADC7,PC[5:0]
AREF
ADC[7:0]
AREF
EXTINT
PD[7:0], PC[6:0], PB[7:0]
PD3, PD2
PCINT[23:0]
INT[1:0]
USART 0
RxD0
TxD0
XCK0
PD0
PD1
PD4
TC 1 (16-bit)
PB1, PB2
PD5
PB0
OC1A/B
T1
ICP1
TWI 0
SDA0
SCL0
PC4
PC5
TC 2 (8-bit async)
PB3
PD3
OC2A
OC2B

AC Analog Comparator

- Blok Analogni komparator AC ugradjen je u ATmega328
- Analogni komparator ima dva ulaza:
  - neinvertujući (+) i
  - invertujući (-)
- AC upoređuje naponske vrednosti na neinvertujućem (AIN0) i invertujućem pinu (AIN1)
- Izlaz iz komparatora ACO (Analog Comparator output) postavlja se prema

$$U_{ACO} = \begin{cases} +5, & U_{AIN0} \geq U_{AIN1} \\ 0, & U_{AIN0} < U_{AIN1} \end{cases}$$

Blok šema AC


BANDGAP REFERENCE
ACBG
AIN0
AIN1
ACME
ADEN
ADC MULTIPLEXER OUTPUT(1)
VCC
ACD
+
-
INTERRUPT SELECT
ACIS1
ACIS0
ACIE
ANALOG COMPARATOR IRQ
ACI
ACIC
TO T/C1 CAPTURE TRIGGER MUX
ACO

Izvori signala za komparaciju

- Analogni signali za komparaciju mogu se dovesti
  - spolja (pinovi AIN0 i AIN1)
  - selekcijom 1 od 8 spoljašnjih signala preko ADC multipleksera (ADC MULTIPLEXER OUTPUT)
  - iz unutrašnjeg referentog naponskog generatora (BANDGAP REFERENCE)
- Selekcija ulaznih signala ostvaruje se pomoću upravljačkih registara

Selektovanje signala za komparaciju

Table 27-1. Analog Comparator Multiplexed Input

ACME	ADEN	MUX[2:0]	Analog Comparator Negative Input
0	x	xxx	AIN1
1	1	xxx	AIN1
1	0	000	ADC0
1	0	001	ADC1
1	0	010	ADC2
1	0	011	ADC3
1	0	100	ADC4
1	0	101	ADC5
1	0	110	ADC6
1	0	111	ADC7

Izlazni signal AC

- Izlazni signal i z komparatora ACO postavlja peti bit u ACSR registru.
- Moguće je programski čitati ACO bit i, u zavisnosti od logičkog stanja, vršiti grananje u programu.
- ACO signal se može voditi na ulaz T/C 1, čime se omogućava programsko brojanje.
- ACO signal se može koristiti za aktiviranje prekida
- Aktiviranje može biti preko opadajuće, rastuće ili istovremeno i opadajuće i rastuće (blok INTERRUPT SELECT)

Analog Comparator Control and Status Register

Name: ACSR
Offset: 0x50
Reset: N/A
Property: When addressing as I/O Register: address offset is 0x30

Bit	7	6	5	4	3	2	1	0
	ACD	ACBG	ACO	ACI	ACIE	ACIC	ACIS1	ACIS0
Access	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 – ACD: Analog Comparator Disable
When this bit is written logic one, the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. This will reduce power consumption in Active and Idle mode. When changing the ACD bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

Bit 6 – ACBG: Analog Comparator Bandgap Select
When this bit is set, a fixed bandgap reference voltage replaces the positive input to the Analog Comparator. When this bit is cleared, AIN0 is applied to the positive input of the Analog Comparator. When the bandgap reference is used as input to the Analog Comparator, it will take a certain time for the voltage to stabilize. If not stabilized, the first conversion may give a wrong value.

Bit 5 – ACO: Analog Comparator Output
The output of the Analog Comparator is synchronized and then directly connected to ACO. The synchronization introduces a delay of 1 - 2 clock cycles.

Analog Comparator Control and Status Register

Bit 4 – ACI: Analog Comparator Interrupt Flag
This bit is set by hardware when a comparator output event triggers the interrupt mode defined by ACIS1 and ACIS0. The Analog Comparator interrupt routine is executed if the ACIE bit is set and the I-bit in SREG is set. ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logic one to the flag.

Bit 3 – ACIE: Analog Comparator Interrupt Enable
When the ACIE bit is written logic one and the I-bit in the Status Register is set, the Analog Comparator interrupt is activated. When written logic zero, the interrupt is disabled.

Bit 2 – ACIC: Analog Comparator Input Capture Enable
When written logic one, this bit enables the input capture function in Timer/Counter1 to be triggered by the Analog Comparator. The comparator output is in this case directly connected to the input capture front-end logic, making the comparator utilize the noise canceler and edge select features of the Timer/Counter1 Input Capture interrupt. When written logic zero, no connection between the Analog Comparator and the input capture function exists. To make the comparator trigger the Timer/Counter1 Input Capture interrupt, the ICIE1 bit in the Timer Interrupt Mask Register (TIMSK1) must be set.

Analog Comparator Control and Status Register

Bits 1:0 – ACISn: Analog Comparator Interrupt Mode Select [n = 1:0]
These bits determine which comparator events that trigger the Analog Comparator interrupt.

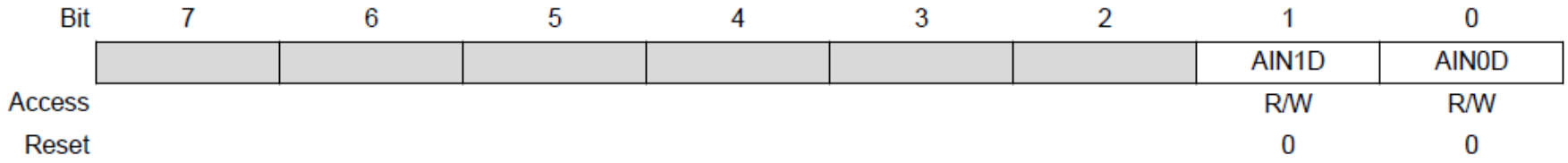
Table 27-3. ACIS[1:0] Settings

ACIS1	ACIS0	Interrupt Mode
0	0	Comparator Interrupt on Output Toggle.
0	1	Reserved
1	0	Comparator Interrupt on Falling Output Edge.
1	1	Comparator Interrupt on Rising Output Edge.

When changing the ACIS1/ACIS0 bits, the Analog Comparator Interrupt must be disabled by clearing its Interrupt Enable bit in the ACSR Register. Otherwise an interrupt can occur when the bits are changed.

27.3.3. Digital Input Disable Register 1

Name: DIDR1
Offset: 0x7F
Reset: 0x00
Property: -



Bit	7	6	5	4	3	2	1	0
							AIN1D	AIN0D
Access							R/W	R/W
Reset							0	0

Bit 1 – AIN1D: AIN1 Digital Input Disable

Bit 0 – AIN0D: AIN0 Digital Input Disable

When this bit is written logic one, the digital input buffer on the AIN1/0 pin is disabled. The corresponding PIN Register bit will always read as zero when this bit is set. When an analog signal is applied to the AIN1/0 pin and the digital input from this pin is not needed, this bit should be written logic one to reduce power consumption in the digital input buffer.

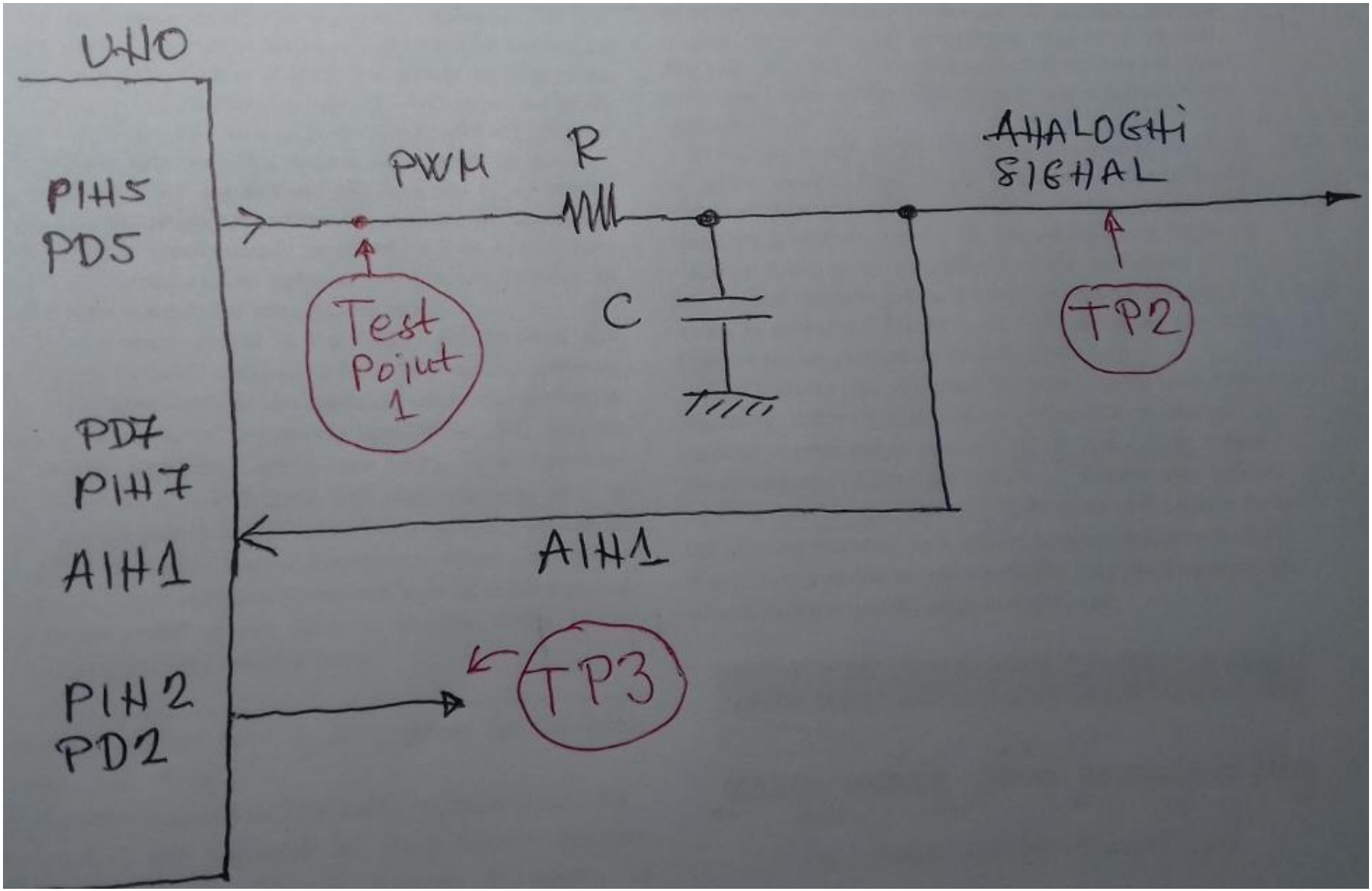
Primer

- Na slici (naredni slajd) prikazana je električna šema veze RC komponenata na Arduino UNO.
- Na pinu 5 (PD5 pin ATmega 328) generisati PWM signal sa faktorom ispune 50%.
- RC filtar će vršiti NF filtriranje PWM signala i, na taj način generisati analogni eksponencijalni signal (punjenje i pražnjenje kondenzatora).
- Eksponencijalni signal vodi se na pin 7 (AIN1 ulaz AC).

Primer

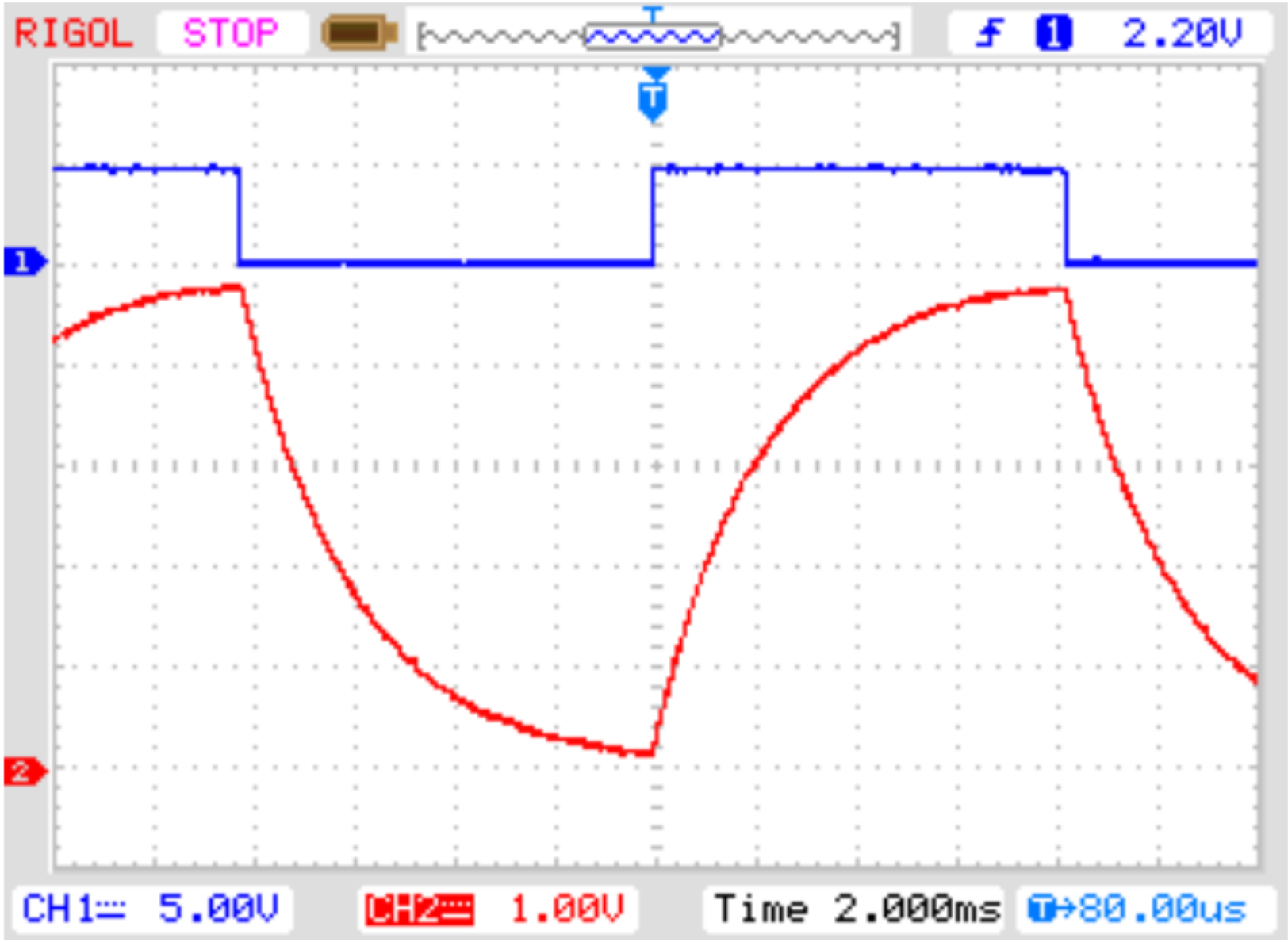
- Napisati program kojim se
- generiše PWM signal ,
- vrši komparacija eksponencijalnog signala i signala sa naponskog referentnog izvora,
- signal sa izlaza komparatora (odnosno njegove kopije u ACSR registru) proslediti na pin 2 (PD2).
- Na električnoj šemi crvenom bojom su označena mesta gde se vrši merenje signala pomoću digitalnog osciloskopa (Test Point 1, 2 i 3)

Primer

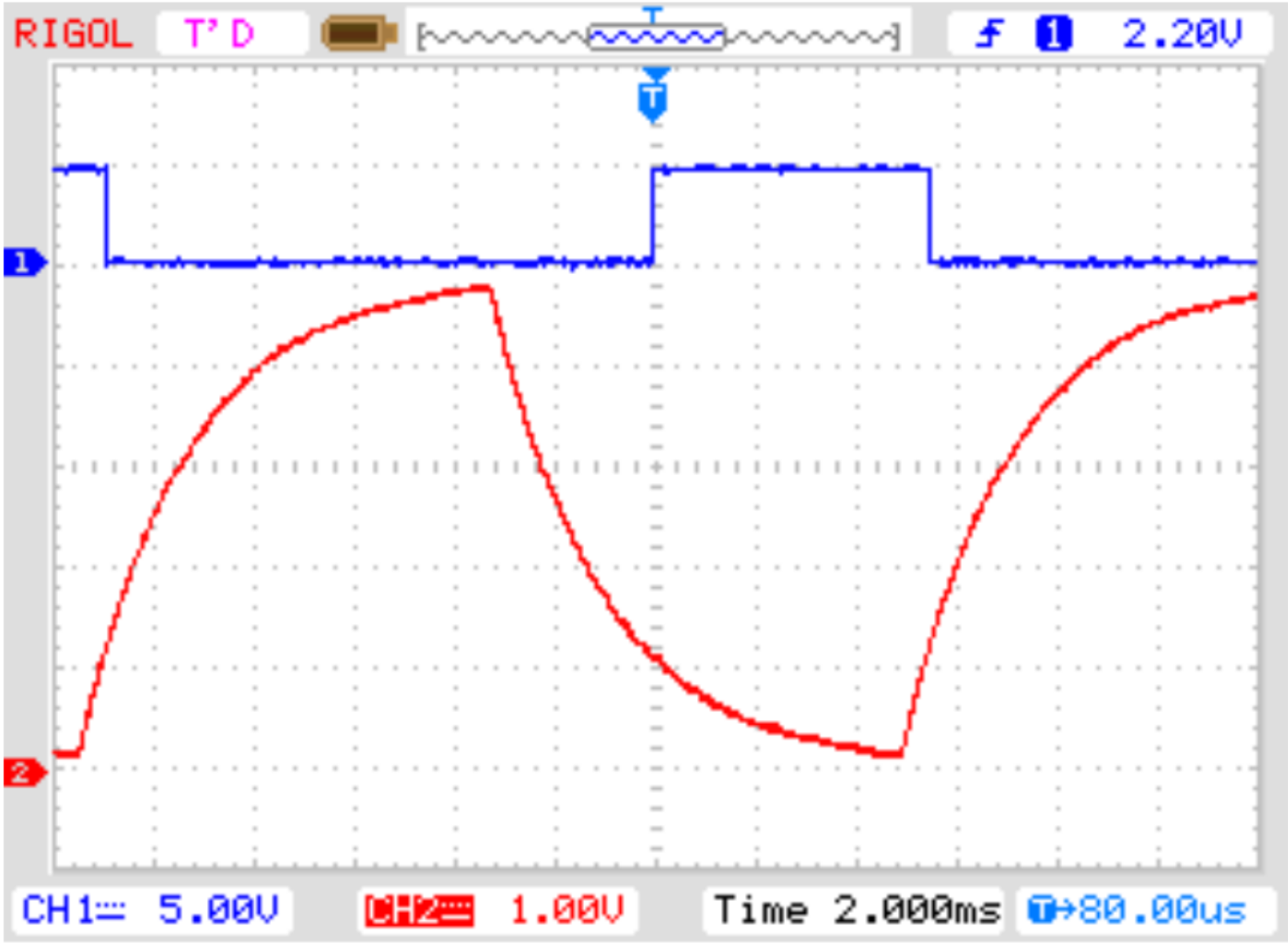

UNO
PIN5
PD5
PWM
R
ANALOGNI
SIGNAL
Test
Point
1
C
TP2
PD7
PIN7
AIN1
AIN1
PIN2
PD2
TP3

```
const byte AC_OUT_TP3 = 2;
const byte PWM_TP1 = 5;
const byte AIN1_TP2 = 7;
unsigned char ch = 0x00;

void setup()
    {
    pinMode(PWM_TP1, OUTPUT);
    pinMode(6,OUTPUT);
    TCCR0A=0;              //resetovanje registra TCCR0A
    TCCR0B=0;              //resetovanje registra TCCR0B
    TCCR0A=0b10100011;     // fast pwm mode
    TCCR0B=0b00000101;     // prescaler 1
    OCR0A=127;             //sirina impulsa na pinu 6
    OCR0B=127;             // sirina impulsa na pinu 5
    ACSR = 0b01000000;
    pinMode(AIN1_TP2, INPUT);
    pinMode(AC_OUT_TP3, OUTPUT);
    }

void loop()
    {
    ch = ACSR & (1 << 5);
    if (ch == 0x00)
        {
        digitalWrite (AC_OUT_TP3, LOW);
        }
    else
        {
        digitalWrite (AC_OUT_TP3, HIGH);
        }
    }
```

Test Point 1 i 2



Test Point 3 i 2



Analiza

- Sa dijagrama se vidi da je promena signala na izlazu komparatora na nivo 1V, što je definisano naponom iz internog referentnog signala koji je povezan na neinvertujući ulaz analognog komparatora.

- **HVALA NA PAŽNJI**